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GB 2034547 A WO 85/02042 A1 US 5184302 A
US 5107427 A

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(54) **Monitoring the measured data acquisistion in an engine control unit**

(57) Measuring device 20 inputs a signal at A1 to A/D converter 12 of arithmetic unit 10 and measuring devices 38 and 40 input signals to A2 via multiplexer 32 under the control of unit 10. The performance of converter channel A2 and multiplexer 32 can be monitored by the arithmetic unit 10 using reference voltage signal UT which is transmitted through the multiplexer via lines 30, 42. The performance of channel A1 can be monitored by unit 10 issuing "high" signal Px, to switch comparator 24 and transmit a "low" reference value of signal UADC which replaces the signal from device 20.

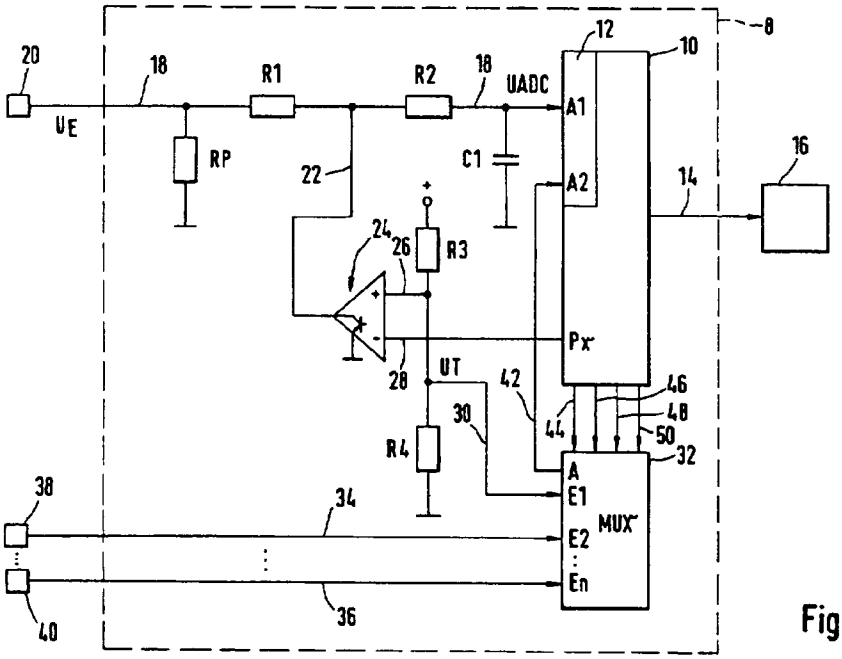

Fig.1

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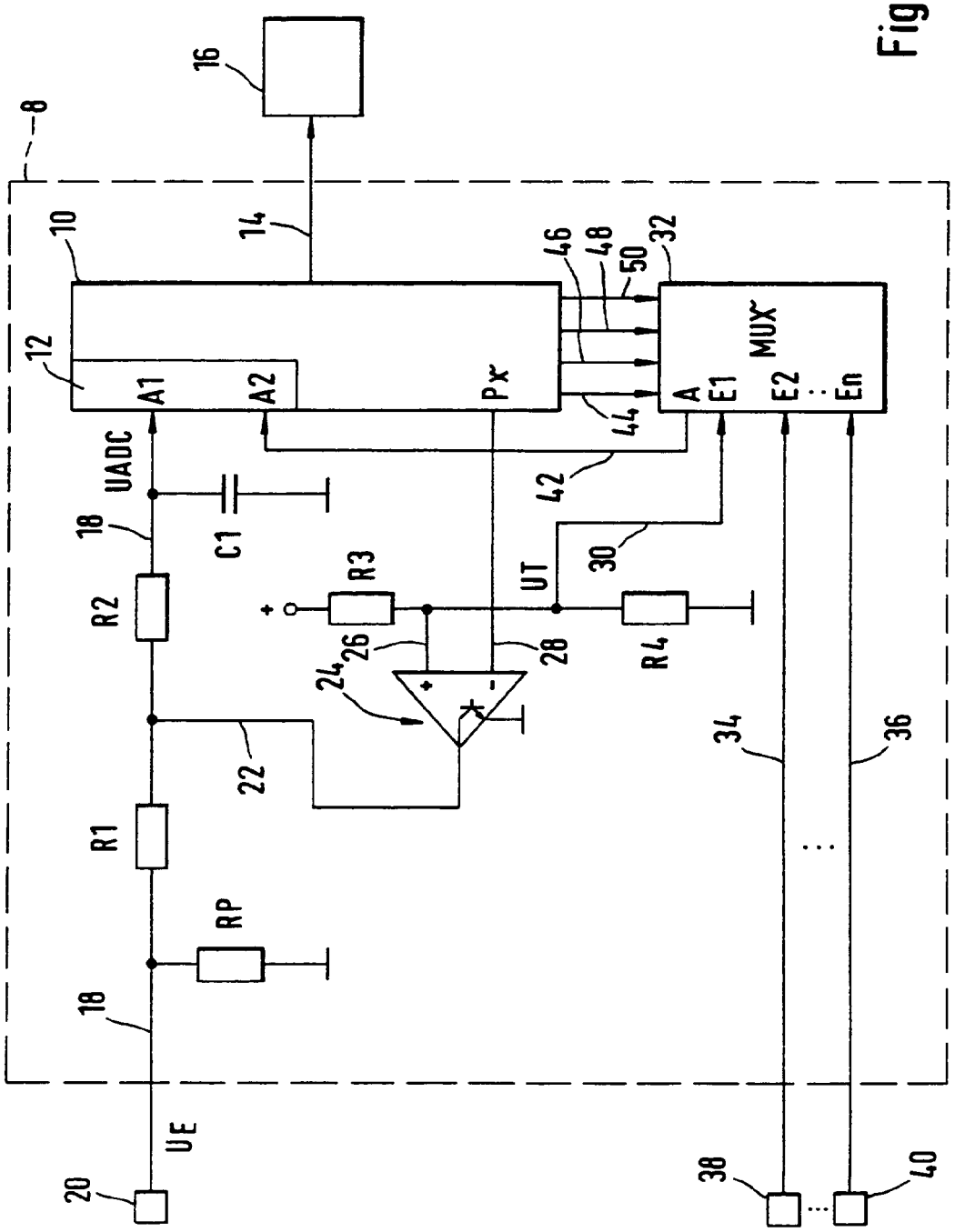

8
16
14
10
12
A1
A2
Px
46
48
50
32
MUX
A
E1
E2
En
44
42
30
UADC
18
C1
R2
R3
UT
R4
26
28
24
22
R1
RP
34
36
UE
20
38
40

Fig.1

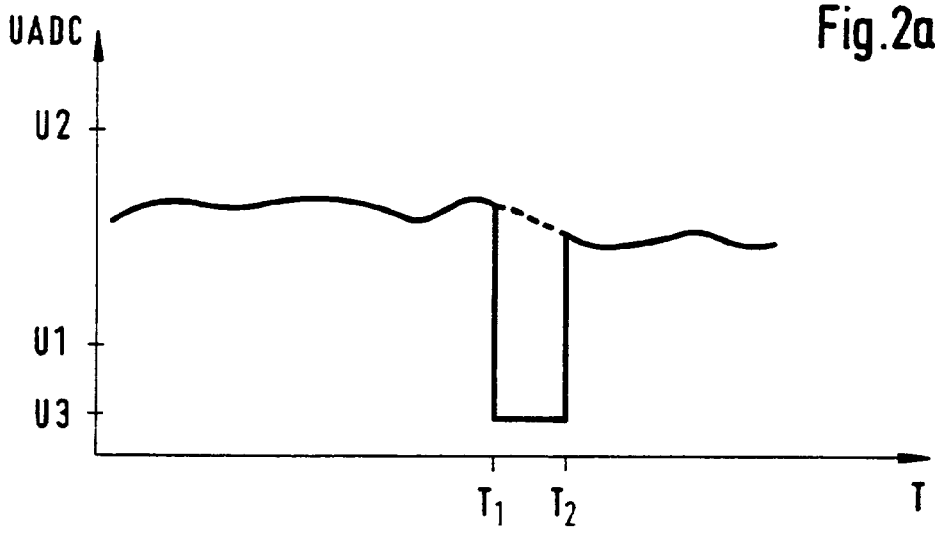


Fig.2a

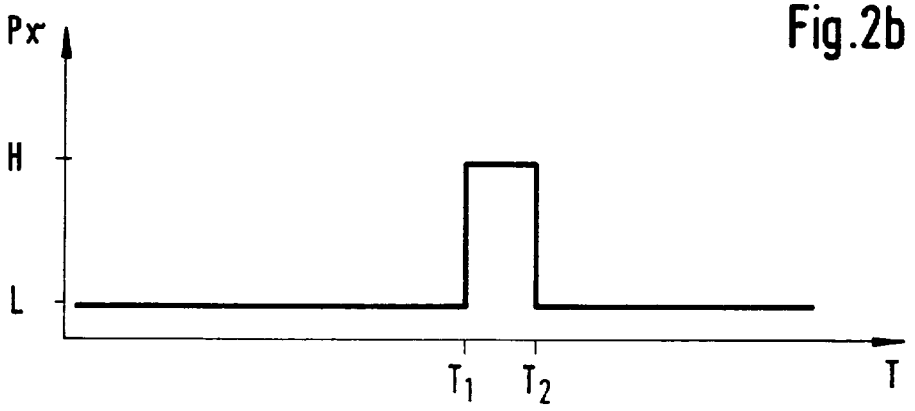


Fig.2b

Fig.3

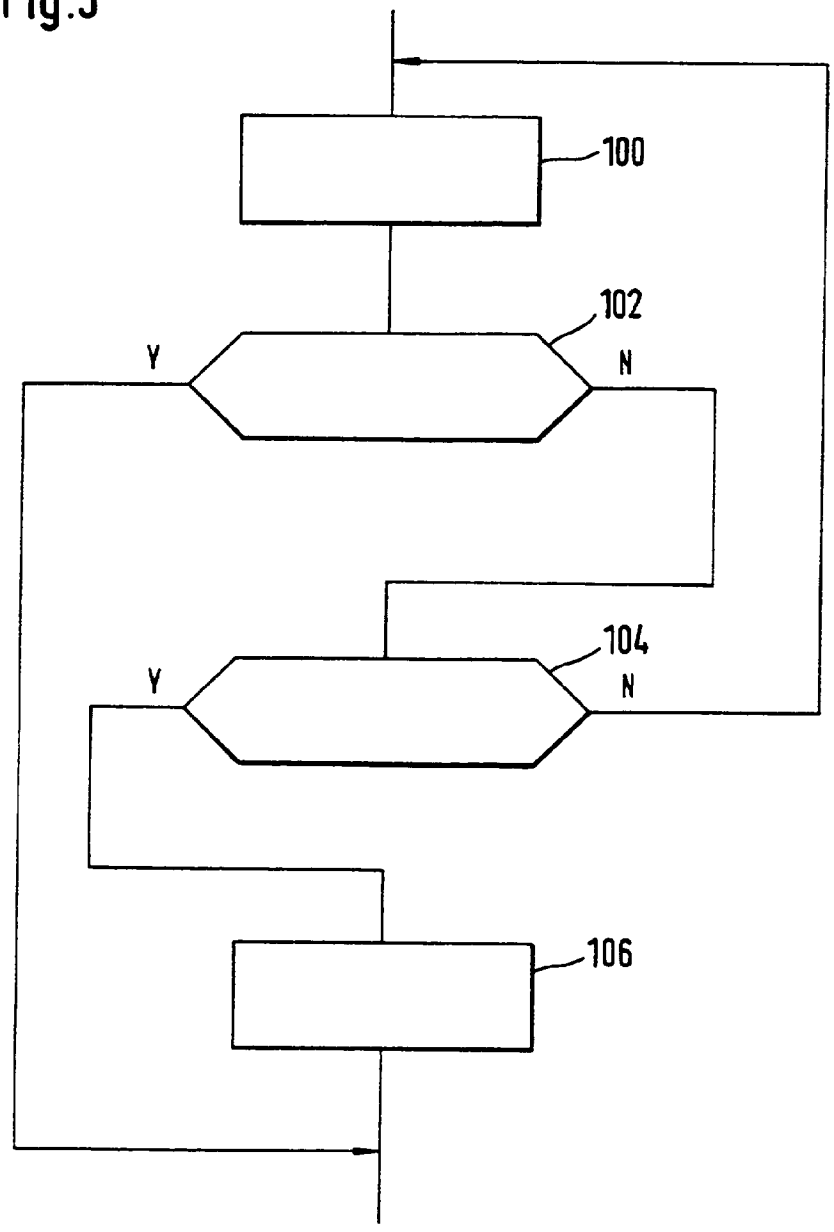
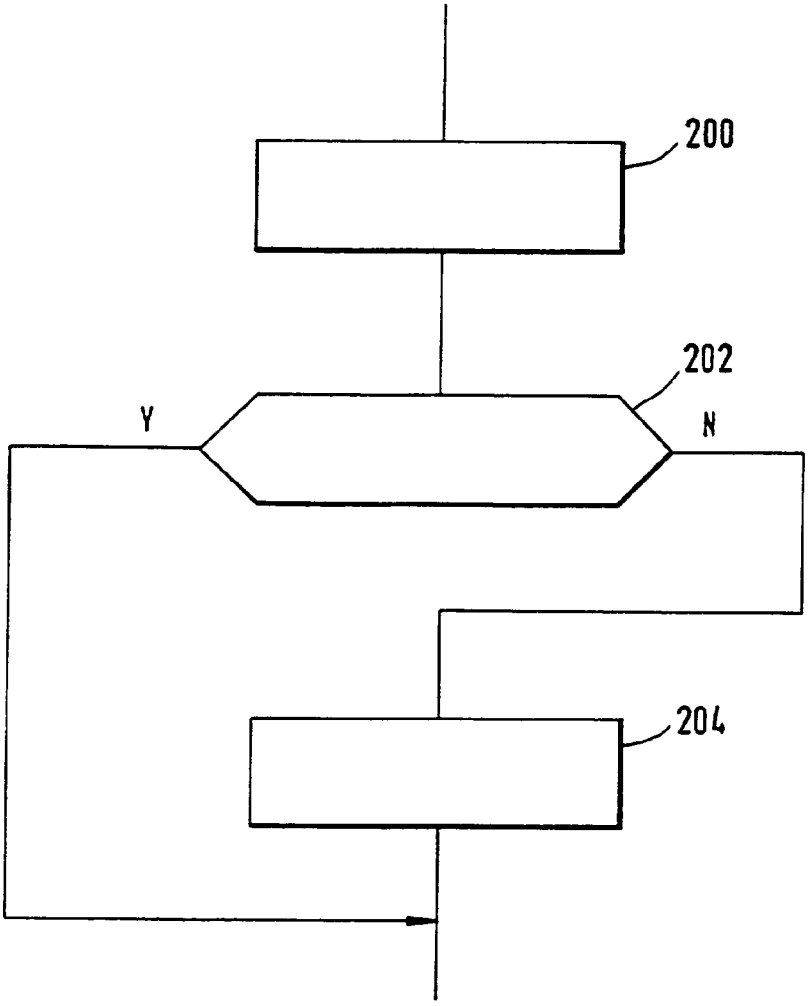


Fig. 4



Process and device for monitoring the measured data acquisition in an engine control unit

Prior Art

The invention concerns a process and a device for monitoring the measured data acquisition in an engine control unit according to the preambles of the independent patent claims.

One such process and one such device is disclosed by DE-OS 36 21 937 (US patent 5, 107, 427). In that document the performance characteristic of the power controller, which is acquired by a measuring device, is influenced for fault detection in the area of the measured data acquisition of an electronic power controller, in particular for detection of faults in A/D interfaces or the channels of a multiplexed A/D converter of the electronic control unit of the power control system. This is achieved by disconnecting the earth lead of the position transmitter, in the form of a potentiometer, of the accelerator pedal and/or of a throttle valve, by means of a switching device that can be actuated by the control unit. A fault condition is identified if the measured variable registered by the measuring device in the disconnected state exceeds specified limiting values or values derived from the measuring device's supply voltage which has been read in.

It has been shown that a relatively long time occurs, especially due to the tolerances of the measuring devices and the supply leads to the control unit of the monitoring cycle, during which engine control cannot be implemented. Furthermore, additional circuit measures are required in the area of the switching device, particularly with respect to the resistance of the switching device to short-circuits in relation to the

battery voltage or supply voltage, respectively. Moreover, due to the known procedure, the function of the channels of an analogue/digital converter are certainly checked, but not that of an upstream multiplexer.

The object of the invention is to specify measures which offer monitoring of the measured data acquisition which is as accurate as possible and which does not influence engine control or only slightly so.

This is achieved by the characterising features of the independent claims.

EP-354 269 A1 proposes a process and a circuit arrangement for monitoring the contact resistance of a potentiometer. Here the actual contact resistance of the potentiometer is calculated at predetermined time intervals by the arithmetic unit from the signal line level connected to earth via a switching device and from the variables available in the arithmetic unit with respect to potentiometer setting, voltage in the connected state, as well as supply voltage. Measures to monitor the measured data acquisition are not described, so that a fault state in the area of the A/D converter of the arithmetic unit leads to defective operation of the power control.

Advantages of the invention

The solution according to the invention permits reliable and precise monitoring of a multiplexer connected upstream of an A/D converter, its input variables and/or the A/D channel which receives its output.

The solution according to the invention allows the current status of the A/D converted voltage values of the A/D channel to be tested.

The solution according to the invention provides a circuit arrangement for disconnecting the useful signal, which enables rapid and precise checking of the analogue/digital converter of an arithmetic unit.

It is particularly advantageous that a simple circuit arrangement is employed without a large outlay on components.

It is particularly advantageous that a signal, which is used to monitor a second channel of the A/D converter and/or to monitor an upstream multiplexer, is derived from the circuit arrangement.

It is particularly advantageous that in normal operation only a small residual current flows through the circuit arrangement and due to the rapid disconnection only very little interference to the useful signal is to be expected.

Further advantages are revealed in the following description of exemplary embodiments or in the dependent claims, respectively.

Drawing

The invention is explained in further detail below with the aid of the embodiments illustrated in the drawing. Figure 1 shows a circuit arrangement for disconnecting a useful signal for checking an analogue/digital converter. Figure 2 describes the main signal waveforms which occur as a result of this. A flow chart which represents a program used to monitor an A/D channel is outlined in Figure 3. Figure 4 illustrates a flow chart which exemplifies a program for monitoring a second A/D channel and/or an upstream multiplexer.

Description of exemplary embodiments

Figure 1 illustrates an arithmetic unit 10 forming part of an electronic control unit 8, which has an analogue/digital converter 12 with at least two input channels A1 and A2. The arithmetic unit 10 controls the power of the engine of a vehicle via at least one output line 14 in accordance with the implemented programs. In the preferred exemplary embodiment a power control element 16, preferably a throttle valve, is set in relation to the driver's wishes which are detected by a position transmitter on the accelerator pedal. An input line 18, which runs from a measuring device 20 for detecting the accelerator pedal position, i.e. the driver's wishes, is assigned to a first input channel of the ADC 12.

The input circuit of the first ADC channel is constructed as follows. The line 18 carries the measured variable UE (accelerator pedal position) from the measuring device 20 to the control unit 8. At this point it is led via a first resistor R1 and a second resistor R2 to the input A1. A resistor RP is connected from the line 18 to earth between the input of the control unit and the resistor R1. A line 22 is connected to the line 18 between the resistors R1 and R2. A capacitor C1 is connected to earth between the resistor R2 and the input A1. The measuring voltage UADC appears at the input A1.

The line 22 is the output line of a comparator 24. Depending on its input signals, the comparator 24 outputs a "low" signal via the line 22 or open-circuits the line 22. This function of the comparator 24 is symbolised by a switching device shown in the comparator 24. A line 26 is led to the positive input of the comparator 24, and a line 28 which runs from an output PX of the arithmetic unit 10, is led to the negative input. The line 26 supplies the divider voltage of a voltage divider consisting of the

resistors R3 and R4, the resistor R3 being connected to the positive supply and the resistor R4 to earth.

Furthermore, the divider voltage is supplied via a line 30 to the input E1 of a multiplexer 32. At its inputs E2 to En the multiplexer 34 receives input lines 34 to 36, which run from measuring devices 38 to 40 for the detection of additional performance data required for engine control. These performance data are fed in multiplexed form to the arithmetic unit for evaluation. Examples of such data are engine temperature, inlet air temperature, air pressure, etc. A line 42 which is led to the second input A2 of the ADC 12 is connected to the output A of the multiplexer. The multiplexer 32 is controlled by the arithmetic unit 10 via control lines 44, 46, 48 and 50.

The circuit arrangement illustrated in Figure 1 ensures intermittent monitoring of the AD converter of the arithmetic unit 10. For this, at an analogue input (A1) the actual measuring voltage UADC, which in normal operation varies over a predetermined range U1 to U2, is taken to earth or is set to a low voltage level, respectively, for a definite time by an external circuit. The effect of this action is that the measuring voltage UADC is taken to a level U3 that is very much lower than the lower level of the measuring signal U1. The level U3 lies well outside the measuring window U2-U1. The arithmetic unit controls this action via the output PX and when the input channel changes checks the voltage that is input to see if it reaches an expected value. In this case the ADC operates normally. Corresponding measures are applied in other exemplary embodiments to the other analogue inputs of the arithmetic unit.

The output of the comparator 24 switches to "low" if the computer outputs a "high" signal via its output PX. The voltage UADC at the input goes to U3. In this case U3

corresponds to the saturation voltage of a switching device which is activated in the comparator. The arithmetic unit 10 checks whether the ADC correctly converts the value of U3 within the tolerances. The useful signal UE cannot be used during this time.

In the preferred exemplary embodiment of an electronic engine power controller, in which the accelerator pedal position is detected by two redundant sensors, it is sensible to influence the useful signal which merely acts to monitor the useful signal controlling the power controller. Further use is then made of the useful signal controlling the power controller.

So that the capacitor C1 used to smooth the analogue signal can be rapidly discharged for the measurement, the value of resistor R2 is made significantly smaller than R1.

The cut-off current of the inhibited comparator is so small that it scarcely distorts the useful signal UE, and furthermore flows to earth (through the transistor in the comparator), so that in the event of a cable break it does not generate any voltage across the resistor RP and thus does not distort the comparison which is carried out to detect a cable break.

This circuit arrangement enables the useful signal to be simply influenced in order to check the AD converter. The circuit is constructed so as to ensure a low residual current and rapid checking of the ADC with consequently only minimal impairment of the useful signal.

Furthermore, the divider voltage UT which is fed to the comparator 24 as a reference voltage, can be used as a reference for continuous checking of an additional analogue

input channel A2. If this analogue input is controlled via a multiplexer, then besides the monitoring of the ADC, monitoring of the correct operation of the multiplexer can also be employed.

The multiplexer 32 is controlled by the arithmetic unit 10 via the control lines, so that various input variables E1 to En can be read in via the input A2 and the output A of the multiplexer. The divider voltage UT is fed as an input variable to one input of the multiplexer (E1 in Figure 1) via the line 30 and read in by the arithmetic unit 10 accordingly. The arithmetic unit 10 then additionally checks the fixed divider voltage in order to monitor the input A1, so as to provide an indication of the operational performance of the multiplexer and of the ADC input A2. Moreover, this method detects whether faults occur at any of the other input signals E2 to En. For example, if overvoltages occur at an input channel of the multiplexer, then all other input channels are affected by cross-talk. This is detected by reading the divider voltage.

Timing diagrams of the main signals are illustrated in Figures 2a and 2b. Figure 2a describes the time characteristic of the useful signal voltage UADC, while Figure 2b illustrates the time characteristic of the output signal PX of the arithmetic unit. The output signal of the arithmetic unit is "low" up to a time T1. This means that the useful signal is not affected. It therefore varies between the voltages U1 and U2 according to the input variable UE. At time T1 the output line of the arithmetic unit 10 is switched to "high". Accordingly, at time T1 the useful signal changes to a level U3 that lies sufficiently below the measuring range U1 to U2. At time T2, on completion of the checking cycle, the output PX of the arithmetic unit is again switched to "low", so that at this time the useful signal again assumes the useful signal value UADC, as shown in Figure 2a.

The check is initiated if selected test conditions are present. For example, these exist in a time condition or are determined via the vehicle's and/or the engine's operating states. Provision can thus be made, for example, for the useful signal to be switched off during the engine starting phase, with the accelerator pedal released, with a substantially constant accelerator pedal position, on expiry of a predetermined operating period or time interval.

To monitor the A/D converter by disconnecting the useful signal, the arithmetic unit 10 has a suitable program which is outlined in the flowchart shown in Figure 3. This program is initiated if the arithmetic unit 10 sets the output PX to "high" level, i.e. if the test conditions apply. In the first step 100, the input voltage UADC is read in and in the following step 102 it is compared to the specified value U3. If the voltage value in the tolerance band equals the predetermined value U3, the test is ended and the output signal PX is again set to "low". In this case the input channel is considered to be operational. If the voltage read in the tolerance band does not correspond to the voltage value U3, a check is made in the following step 104 to see if the test cycle is ended. This is preferably the case after a predetermined time, after which the arithmetic unit again sets the output PX to "low". If this condition is not met, the functional check is repeated with step 100. If the end of the test is reached without the operational capability of the input channel having been determined, an error response is triggered in step 106, which initiates emergency operation in relation to the power controller. The program section is then initiated if the next test condition is present.

The arithmetic unit 10 has a comparable program for checking the second input channel or the multiplexer, respectively. This is outlined in the form of a flowchart in Figure 4. The program described there is initiated at a specified time in synchronism with the control of the multiplexer. If the divider voltage UT is fed via

the multiplexer to the arithmetic unit 10, the program is initiated as shown in Figure 4 and the voltage UT is read in at the first step 200. After that, step 202 checks whether the voltage which is read in within the tolerance band corresponds to the voltage value UT0 set by the resistors R3 and R4. If this is so, the multiplexer or the input channel A2, respectively, is assumed to be operating correctly and the program section is ended, otherwise a corresponding error response, such as limiting the power control, for example, is triggered in step 204. After step 204 the program is ended and is initiated again at the next time point.

In a preferred exemplary embodiment, the error response is only generated when the error has been detected several times in succession or at a certain frequency.

CLAIMS

1. A process for monitoring the measured data acquisition in an engine control unit, an arithmetic unit (10) being provided, which has available at least one input (A2) of an A/D converter (12), to which various input signals are fed via a multiplexer (32), **characterised in that** one of the input signals is a fixed, predetermined reference voltage (UT) that is read in by the arithmetic unit (10) for checking the mode of operation of the multiplexer and/or of the A/D converter (12).

2. Process according to Claim 1, **characterised in that** an error response is generated if the voltage read in and converted via the multiplexer does not correspond to an expected value.

3. Process according to one of the preceding Claims, **characterised in that** the arithmetic unit reads in via a further input (A1) of the A/D converter (12) a measuring voltage (UADC) representing the driver's wishes, said measuring voltage being switched at predetermined times to a specific level for checking the correct conversion at the analogue input (A1).

4. Device for monitoring the measured data acquisition in an engine control unit, having an arithmetic unit (10) which has at least one analogue input (A1) of an analogue/digital converter (12), to which input a useful signal evaluated for engine control is fed via an input line (18), **characterised in that** the output line (22) of a comparator (24) is connected to the input line (18), whereby a "low" signal is generated at

the output by the arithmetic unit (10) via an output (PX), whereupon the input voltage (UADC) at the analogue input (A1) is set to a level that lies outside the measuring voltage range.

5. Device according to Claim 4, **characterised in that** the output line of the arithmetic unit (10) is connected to the negative input of the comparator, while a fixed, predetermined divider voltage (UT) is fed to the positive input.

6. Device according to one of Claims 4 to 5, **characterised in that** the arithmetic unit (10) has at least a second analogue input (A2) to which the output line (42) of a multiplexer (32) is fed.

7. Device, in particular according to Claim 6, **characterised in that** the arithmetic unit (10) has at least a second analogue input (A2) to which the output line (42) of a multiplexer (32) is fed and to said multiplexer is fed in addition to input lines via which further operational data of the engine and/or the vehicle are fed, the divider voltage (UT) of the comparator, which the arithmetic unit (10) reads in for the evaluation of the operational performance of the multiplexer and of the analogue input (A2).

8. Device according to one of Claims 4 to 7, **characterised in that** two resistors (R1, R2) are provided in the input line (18) of the useful signal, between which resistors the line (22) is fed, the value of the resistor (R2) being very much smaller than the resistor (R1).

9. Device according to one of Claims 4 to 8, **characterised in that** furthermore a capacitor (C1) is provided, that is connected to earth between the input (A1) and the resistor (R2).

10. Device according to one of Claims 4 to 9, **characterised in that** the arithmetic unit (10) is used to control the power of the driving unit of a vehicle in relation to the driver's wishes.

11. A process for monitoring the measured data acquision in an engine control unit, substantially as hereinbefore described with reference to the accompanying drawings.

12. A device for monitoring the measured data acquisition in an engine control unit, substantially as hereinbefore described with reference to the accompanying drawings.

The Patent Office

13

Application No: GB 9720330.1 **Examiner:** Michael Prescott
Claims searched: 1-3 **Date of search:** 13 November 1997

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

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Int Cl (Ed.6): F02D 41/22; H03M 1/10

Other: Online: WPI

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
X	GB 2034547 A	(TOKYO SHIBAURA) see page 2 lines 59-80	1, 2
X	WO 85/02042 A1	(SUNSTRAND) see page 15 lines 14-34	1, 2
A	US 5184302	(MITSUBISHI DENKI) whole document	1, 2
X	US 5107427	(ROBERT BOSCH) - referred to in application - see column 2 lines 3-9, column 4 line 56 to column 5 line 24 and column 5 line 58 to column 6 line 8	1, 2

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.